A Roadmap on the Low Power Static Random Access Memory Design Topologies

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Abstract— The increasing demand for more and novel applications in electronics systems have persuaded the semiconductor technology towards scaling of devices to accommodate a large number of circuit component in a single Integrated Circuit. Thus high density and faster chips have become semiconductor industry's requirement. But faster circuits need more power to work properly and hence reduces the battery lifetime. This paper provides a systematic overview of Static Random Access Memory based on semiconductor technology (45,65,130 and180 nm), Bit-Cell type (1T,2T,3T upto 14T), various circuit design techniques (power gating, dual Vth, body biasing, MTCMOS, Sub threshold, etc.) for ultra low power applications, eg. Bio-medical, Wireless sensors, Multimedia applications. Recent trends of shrinking the semiconductor devices into nanometer regime lowers the operating power requirements. This lower operating voltage(Vdd) starts offering other challenges such as speed, stability. It is seen that if speed is increased then power also increases. If access time is decreased , the noise margins also increases. If Vmin is reduced then reliability improves.

Index Terms— Bio-Medical, multimedia, 3-D graphics, wireless sensors

1 INTRODUCTION

SRAM has advantage over DRAM because of its high speed, faster access time, low power dissipation and it doesn't require being refreshed again and again. SRAM is mostly used for cache memory, the memory used on processors and hard drives to store frequently used data and instructions. SRAM is used in a lot of devices where speed is more crucial than capacity.Because of its application in high speed communications and 3-D Graphics systems there is large demand for high speed embedded memories [12]. Battery lifetime specifications drives a great impact on the power consumption requirements of integrated circuits in bio- implantable, wearable, and portable medical devices [32]. Stand by power is a major problem in low power applications. The amount of circuitry on a chip as well as circuitry speed have continued to increase exponentially since the invention of integrated chips. The scaling of CMOS technology has brought several challenges for SRAM designers to meet market demands [37]. To reduce standby leakage following techniques can be used: i To increase threshold voltage NMOS and PMOS are reverse body biased ii To reduce the effective Vdd across the SRAM cell , bias the source (Vs) of the SRAM cell NMOS latch above ground iii In standby mode to turn off the circuits use sleep transistors [42].Various low power methodologies are used e.g. Self reverse bias technique, Multiple Vth technique, Multi threshold-Voltage CMOS (MTCMOS), Multiple body bias, Dual threshold CMOS, Dynamic Vth technique etc. Subthreshold logics are also becoming renounced for ultra-low power applications like portable electronics, medical instruments, and sensor networks where minimum power consumption is the main requirement [45].Various multi voltages schemes are proposed with increased process corners complexity. Depending on the targeted application constraint tradeoffs like power, area, performance and stability are prioritized. The highly power constrained systems require more power for its active mode operations [55]. To achieve high speed, low voltage and smaller area semiconductor circuits and systems are implemented into nano metre regime [67].

2 LOW-POWER SRAM BIT-CELL TOPOLOGIES

This section presents various SRAM Bit-Cell topologies reported so far by various researchers in the domain of semiconductor SRAM design. Here, the bit-cell topologies have been organized in respect with the number of transistors in the SRAM cell and technology. A lot of good work is available in the literature these days. This was a big challenge before us to what to include and what to not. Though we have tried, but the inclusion of all the research paper is not possible in one survey, we have focused on low-power SRAM bit-cell topologies and technologies. Various low power methodologies are used e.g. Self reverse bias technique, Multiple Vth technique, Multi threshold-Voltage CMOS (MTCMOS), Multiple body bias, Dual threshold CMOS, Dynamic Vth technique etc.

TABLE 1: THE 1T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Moselund K.E., Bouvet D., Pott V., Meinen C., Kayal M., and Ionescu A.M., "Punch-through impact ionization MOSFET (PI-MOS): From device principle to applications,"[1]	TCAD	-	-	-	-	punch-through impact ionization MOSFET	High Current Consumption	High temperature stability, less switching activity	Hysteresis width can be optimized by the value of Vds.
Leung Wingyu, Hsu Fu-Chieh, and Jones Mark-Eric, "The Ideal *SoC* Memory: lT-SRAM,"[2]	CMOS 180	-	-	300	-	multi-bank architecture and multi-layer metal interconnect	high-frequency operation, short latency, transparent refresh and soft-error rate	Easy to port, remove process incompatibility, extremely scalable, cost effective	1T-SRAM enables the economic embedding of very large quantities of memory in SoC designs.
Jin Niu, Chung Sung-Yong, Yu Ronghua, Heyns Roux M , Berge Paul R., and Thompson Phillip E., "The Effect of Spacer Thicknesses on Si-Based Resonant Interband Tunneling Diode Performance and Their Application to Low-Power Tunneling Diode SRAM Circuits,"[3]	N channel depletion mode FET	-	-	-	0.5	Si based resonant interband tunneling diodes (RITD)	Temperature change may effect	Low stand by power consumption, increase circuit speed, reduce component count,	Suitable for low power memory applications, Spacer thickness reduced to 16nm, Current density reduced to 0.5A/cm2, peak-to-valley current ratio (PVCR) reduced to 2.2
Glaskowsky Peter N., "MoSys Explains 1T-SRAM Technology Unique Architecture Hides Refresh Makes DRAM Work Like SRAM,"[4]	CMOS	-	-	-	-	Hide refresh technique-DRAM work like SRAM	Area may increase	High speed , high density,	No refreshing is required, No wait state,
Jones Mark-Eric, "1T-SRAM-Q™: Quad-Density Technology Reins in Spiraling Memory Requirements,"[5]	45 CMOS	-	-	-	-	Quad Density Technology	Complex designing	Highly scalable, Reliable, Small size, Cost effective, Enhanced soft error rate, Improved yield	4times higher density than traditional 6T SRAM, Enhanced reliability using Transparent error

									correction

TABLE 2: THE 2T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Somasekhar Dinesh, Ye Yibin, Aseron Paolo, Lu Shih-Lien, Khellah Muhammad, Howard Jason, Ruhl Greg, Karnik Tanay, Borkar Shekhar Y., De Vivek, and Keshavarzi Ali, "2GHz 2Mb 2T Gain-Cell Memory Macro with 128GB/s Bandwidth in a 65nm Logic Process,"[6]	65	-	0.00028000	2000	1.1	Pipelined macro cells	area may increase	Fast cycle time, Faster read operation	retention time =10μs, Array Density 92Mbit/cm2
Meinerzhagen Pascal, Teman Adam, Mordakhay Anatoli, Burg Andreas, and Fish Alexander, "A Sub-VT 2T Gain-Cell Memory for Biomedical Applications,"[7]	180	-	-	-	0.4(sub-Vt)	SUB-VT GAIN-CELL	Capacitive coupling may occur	Good energy efficiency, low power consumption, highly robust	data retention time is higher than data access time

TABLE 3: THE 3T SRAM BIT-CELL TOPOLOGY

Author& Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Ramesh Anisha, Park Si-Young, and Berge Paul R., "90 nm 32x32 bit Tunneling SRAM Memory Array With 0.5 ns Write Access Time, 1 ns Read Access Time and	90 CMOS	-	0.0000183	-	0.5	DualVth, TSRAM(tunneling based static random access memory)	Noise margins may increase	High speed tunneling, low static and dynamic power dissipation, high robustness	Read access time-1ns, Write access time=0.5ns , Array size=32x32 Standby power dissipation of 6x(10)-5

0.5 V Operation,"[8]									mW per cell dynamic power dissipation of 1.8x (10)-7 mW per cell
Wagt van der J. P. A., Seabaugh A.C., and Beam E.A., "RTD/HFET Low Standby Power SRAM Gain Cell,"[9]	HFET/RTD	-	-	-	0.4	Tunneling SRAM using RTD(resonant tunneling diodes), HFET(hetero structure field transistors)	Area overheads may increase	Reduced standby power consumption, more compact, low current density	Reduced standby power reduction=50nW, high speed, access time=0.5ns

TABLE 4: THE 4T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Nod Kenji, Matsui Koujirou , Takeda Koichi, and Nakamura Noritsugu, "A Loadless CMOS Four-Transistor SRAM Cell in a 0.18-um Logic Technology,"[10]	180 CMOS	-	0.0019344	-	1.8	Concept of Loadless CMOS	Tradeoff between cell size and SNM	Cell is compact. High stability, high speed and high density	Cell area is 35% smaller.
Arsovski Igor, Chandler Trevis and Sheikholeslami Ali, "A Ternary Content-Addressable Memory (TCAM) Based on 4T Static Storage and Including a Current-Race Sensing Scheme,"[11]	180 CMOS	-	0.01754	-	1.2	Match-line (ML) sense scheme	Bitline can't be high for a long period of time	Increase in density	Power consumption is less.
Noda K., Matsui K., Ito S., Masuoka S., Kawamoto H., Ikezawa N., Takeda K., Aimoto Y., Nakamura N., Toyoshima H., Iwasaki T., and Horiuchi T., "An Ultra-High-Density High-speed Loadless Four-Transistor SRAM Macro with a Dual-Layered Wisted Bit-Line and a Triple-Well Shield,"[12]	180 CMOS	-	0.0019344	400	1.8	Dual-layered twisted bit-line,triple well shielding	Memory capacity is less than embedded DRAM macros	Access speed and reliability is increased	Access time = 2.35 ns. Bit-line signal delay is reduced by 20-25%. SNM > 400 mV

Takeda K., Aimoto Y., Nakamura N., Toyoshima H., Iwasaki T., Noda K., , Matsui K., Itoh S., Masuoka S., Horiuchi T., Nakagawa A., Shimogawa K., and Takahashi H., "A 16-Mb 400-MHz Loadless CMOS Four-Transistor SRAM Macro,"[13]	180 CMOS	-	54.08	400	1.8	Uses end-point dual-pulse drivers, wordline-voltage-level compensation circuit and all-adjoining twisted bit-line scheme	Smaller storage-node capacitance and lower load-element current	Accurate timing control, stable data retention, bit-line coupling capacitance reduced, high speed access and smaller size	Size is 66% of Coventional 6T SRAM. Access time = 2.5 ns
Yang Jinshen, and Chen Li,"A New Loadless 4-Transistor SRAM Cell with a 0.18 µm CMOS Technology,"[14]	180 CMOS	-	-	-	1.8	Bitlines are precharged to ground instead of V_{DD}	Tradeoff between the cellsize and cell stability. Node which is storing logic high can't retain its full swing value because it is floating.	Consumes less power and less area	SNM = 446 mV, Cell layout size is 15% smaller. Highly stable when cell ratio=3. Used in high speed and high density SRAMs.
Giraud B., Amara A., and Vladimirescu A., "A Comparative Study of 6T and 4T SRAM Cells in Double-Gate CMOS with Statistical Variation,"[15]	32 CMOS	-	-	-	1.2	Driverless (DL) SRAM cell	An extra back gate is required	Operating characteristics are improved, stability improved in read and retention mode, less access time	SNM > 350 mV Access time decreased by 50% Area decreased by 30%
Batude P., Jaud M-A., Thomas O., Clavelier L., Pouydebasque A., Vinet M., Deleonibus S., and Amara A, "3D CMOS Integration:Introduction of Dynamic coupling and Application to Compact and Robust 4T SRAM,"[16]	TCAD	-	-	-	1.1	3D Integration Technology	Higher TB is required	Stability and surface density increases, balance between SNM and RNM improved	Leakage current =10 pA/µm RNM = 320 mV SNM = 150 mV Density Gain =16.4%

Mazreah Azizi A., Sahebi Reza M., Manzuri Taghi M., Hosseini Javad S., "A Novel Zero-Aware Four-Transistor SRAM Cell for High Density and Low Power Cache Application,"[17]	65 HSPICE	-	-	-	1.2	Uses two word-lines and one pair bit-line	Average leakage current is 15% greater	High density and low power, retains its data with leakage current and positive feedback without refresh cycle	Average delay access is 30% smaller. Average dynamic energy consumption is 45% smaller. SNM = 0.35 V
R Sandeep, Deshpande Narayan T, and Aswatha A R, "Design and Analysis of a New Loadless 4T SRAM Cell in Deep Submicron CMOS Technologies,"[18]	130 CMOS, 90 CMOS, 65 CMOS	-	-	333.33	1.5 (130 CMOS), 1.2 (90 CMOS) and 1.1 (65 CMOS)	Bit-lines are precharged to ground	Read Access time is greater	Less power and less area, high stability	Capacitance of each bitline = 20 fF Load = 20 fF
Fan Ming-Long, Wu Yu-Sheng , Hu Vita Pi-Ho, Hsieh Chien-Yu, Su Pin, and Chuang Ching-Te, " Comparison of 4T and 6T FinFET SRAM Cells for Subthreshold Operation Considering Variability—A Model-Based Approach,"[19]	32 FinFET	-	-	-	0.4	Model-based approach to consider impact of device variation on stability	-	Better nominal READ static noise margin (RSNM)	Area reduced by 25%.
Degalahal V., Vijaykrishnan N., and Irwin M. J., "Analyzing Soft Errors in Leakage Optimized SRAM Design,"[20]	70 HSPICE	-	-	-	No V_{DD}	4T SRAM without V_{DD}	Between optimizing leakage power and improving immunity to soft error	Leakage and area reduction	Leakage reduced by 60-80% Advantage in area by 12-33%

TABLE 5: THE 5T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Tran Hiep, "Demonstration of 5T SRAM And 6T Dual-Port RAM Cell Arrays,"[21]	600 CMOS	-	-	-	2	Single bitline SRAM cell	-	Can operate at dual-port memory over a wide voltage supply range,improved cell size	Can be used in high density SRAM. Can be implement in ASIC design.
Wieckowski M., and Margala M., "A Novel Five-Transistor (5T) Sram Cell For High Performance Cache," [22]	180 TSMC CMOS	-	0.0067	-	1.8	Based on 7T current-mode cell	-	High-speed, Low-power. Optimization in transistor sizes.	57%enhancement in speed, 12% power reduction and 6% area reduction.
Mohan Nitin and Sachdev Manoj, "Novel Ternary Storage Cells And Techniques For Leakage Reduction In Ternary Cam,"[23]	180 CMOS	-	-	-	1.8	Ternary Content Addressable Memories (TCAM)	Unused state can't be stored in cell	Leakage reduction, high speed, smaller area	Leakage decreased by 32-40%.
Cosemans S., Dehaene W., and Catthoor F., "A Low-Power Embedded SRAM for Wireless Applications,"[24]	180 CMOS	-	0.69	250	1.6	Short buffered bitlines & memory databus, Read operation using dynamic stability, Low-Swing Write Using Shared Low-Swing Receivers, and Distributed Decoder	Large part of die used for on-chip signal monitoring circuits	Energy per access is reduced, area reduced	Active power consumption reduced by factor of 2. Energy per access reduced to 54% Energy = 9.5 pJ Delay = 0.74 ns
Wieckowski M., and Margala M., "A Portless SRAM Cell Using Stunted Wordline Drivers,"[25]	180 CMOS	-	0.00877	-	1.8	Portless concept in an isolated test cell	Some percentage of current ratios in process results in slower operation & reduce efficiency	Higher SNM, less leakage, cell area reduced	Static noise margin increased by 22%. Leakage decreased by 14%

Mazreaht Arash Azizi, Shalmani Mohammad Taghi Manzuri, Noormande Reza, and Mehrparvar Ali, "A Novel Zero-Aware Read-Static-Noise-Margin-Free SRAM Cell for High Density and High Speed Cache Application,"[26]	250 CMOS	-	0.01961	-	2.5	Loop-cutting strategy, use one word-line and one bit-line during read/write operation	-	Data is retained with leakage current and positive feed-back without refresh cycle	Cell size decreased by 18%. Average delay is reduced by 20%. Average leakage current is 8% greater.
Nalam S., and Calhoun Benton H., "Asymmetric Sizing in a 45nm 5T SRAM to Improve Read Stability over 6T,"[27]	45 CMOS	-	-	-	0.5	Novel asymmetric sizing approach to increase read ability	Area and Write Noise Margin	Robust read operation	Read stability and improved writability through write assist techniques.

TABLE 6: THE CONVENTIONAL 6T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Narasimhan S. ,Chiel H.J., and bhunia S., "Ultra-low-power and Robust Digital-Signal-Processing Hardware for Implantable Neural Interface Microsystems,"[28]	70 HSPICE	10	0.21	33.33	0.6	Preferential Design,NSPalgo,power gating,voltage scaling	Delay overheads may increase	Improved total energy, highrobustness, high yield	Yield-79.94% Energy = 106.56 pJ Delay = 4.39 ns
Narasimhan S., and Bhunia Swarup, "Ultralow-Power and Robust Embedded Memory for Bioimplantable Microsystems,"[29]	45 HSPICE	-	0.00025600	0.00025600	0.8	Power gating technique	Noise margins may increase	Low energy dissipation,betterarea, high robustness	Array size-(64x80) Noise margin-Read=209 Write=420 Hold=383 It is 611x faster and 1.4x denser than subThreshold design. Energy = 33.72 pJ Delay = 0.37 ns

Elakkumanan Praveen,Thondapu Charan, and Sridhar Ramalingam, "A Gate Leakage Reduction Strategy For Sub-70nm Memory Circuits,"[30]	65 BPTM	_	_	_	0.8	N-controlled SRAM using dual Vth (Dynamic voltage scaling)	1-3% less performance.	Better leakage savings	60% reduction in gate leakage
Hua Chung-Hsien, Cheng Tung-Shuan, and Hwang Wei, "Distributed Data-Retention Power Gating Techniques for Column and Row Co-Controlled Embedded SRAM,"[31]	130 CMOS	-	-	-	1	Column and row co-controlled power gated SRAM	Extra AND gate delay	High robustness	SNM-340 mV, active power reductions (PDP) 32-bit-49%, 16-bit-75% 8-bit -93%,area overhead-8.1%
Sridhara Srinivasa R., DiRenzo Michael, Lingam Srinivas, Lee Seok-Jun, Blázquez Raúl, Mxey Jay, Ghanem Samer, Lee Yu-Hung, Abdallah Rami, Singh Prashant, and Goel Manish, "Microwatt Embedded Processor Platform for Medical System-on-Chip Applications,"[32]	130 CMOS	5nW/kHz(0.5) 19Nw/kHz(0.1)	1.95 um sq bit cell or 1.3mm sq	<1mhz	0.5- 1	Differential SRAM,FFT accelerator	Leakage power,dynamicpower,memory bandwidth ,run time	Less leakage, more reliable	90% effective dc-dc converter, performance 7KHz(0.5v), 5MH(1v), Leakage power 7nW(0.3v), density of SRAM-32kb Energy = 100 nJ
Kulkarni Jaydeep P., and Roy Kaushik, "Ultralow-Voltage Process-Variation-Tolerant Schmitt-Trigger-Based SRAM Design,"[33]	130 CMOS	-	1.063	270 kHz	300 mV	Schmitt-Trigger (ST)-SRAM with Feedback mechanism	Bit cell area increases 2x.	better read-stability as well as better write-ability,	1.6 x higher read static noise margin, 2x higher write-trip-point, Leakage current-0.372Ua
Rooseleer Bram, Cosemans Stefan, and Dehaene Wim, "A 65 nm, 850 MHz, 256 kbit, 4.3 pJ/access, ultra low leakage power memory using dynamic cell stability and a dual swing data link,"[34]	65 CMOS	25.2	0.48	850	1.0	Dual swing data link on the GBLs, High threshold voltage cells, Dynamic decoder with merged address latches	Noise margins may increase	ultra low leakage power and very low active energy consumption, improved stability, high speed, improved robustness	Memory size -256 kbit, Wordlength -32 bit, Cell type- L = 60 nm, W = 120 nm Energy = 4.3 pJ/access

Bansal Aditya, Mukhopadhyay Saibal, and Roy Kaushik, "Device-Optimization Technique for Robust and Low-Power FinFET SRAM Design in NanoScale Era,"[35]	50 FinFET	-	-	-	1.0	FinFET	Access time and performance,stability	Minimized leakage current and drain capacitance to on-current ratio, high robustness,	65%SRAM leakage is reduced, improves cell read failure by 200times,Tox-1.2nm
Amelifard Behnam, Fallah Farzan, and Pedram Massoud, "Leakage Minimization of SRAM Cells in a Dual-Vt and Dual-Tox Technology,"[36]	65 HSPICE	-	-	-	1.1	Dual Vt, Dual Tox	Area overheads ,delay	Reduced leakage power dissipation, improved performance	Power dissipation of SRAM array size-64x512 is reduced to 33%. Power dissipation of SRAM array size-32x512 is reduced to 40%. Vth-0.18v
Sharifkhani Mohammad and Sachdev Manoj, "An Energy Efficient 40 Kb SRAM Module With Extended Read/Write Noise Margin in 0.13 um CMOS,"[37]	130 CMOS	-	-	100	0.4 per cell	Virtual ground architecture	Access time may increase	Low leakage current,energy efficient ,improved stability	28% noise margin enhancement, size-40kb, leakage current-27Pa/Cell, area overhead 8%, dynamic data stability management. Energy = 7 pJ
Lakshminarayanan S., Joung J., Narasimhan G., Kapre R., Slanina M., Tung J., Whately M., Hou C-L., Liao W-J., Lin S-C., Ma P-G., Fan C-W., Hsieh M-C., Liu F-C., Yeh K-L., Tseng W-C., and Lu S.W., "Standby PowerReduction and SRAM Cell Optimization for 65nm Technology,"[38]	65 CMOS	-	-	-	1.0	Body biasing technique	Stability issues may arise	Reduced leakage current, improved performance	Fast process corners, improved yield

TABLE 7: THE 7T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Jiao Hailong, and Kursun Volkan, "Low Power and Robust Ground Gated Memory Banks with Combined Write Assist Techniques,"[39]	65 CMOS	-	-	1000	1.2	Multi Threshold CMOS technology	Careful transistor sizing,cell layout optimization	Stronger data stability and lower leakage power consumption	write margin enhanced to 2.75x, write delay reduced to 71.70%, data stability increases by

									2.11x, leakage power consumption reduces by 65.38%. cell layout area is increased upto 26.97%, electrical quality is enhanced by 9.36x
Liu Zhiyu and Kursun Volkan, "Characterization of a Novel Nine-Transistor SRAM Cell,"[40]	65 CMOS	-	-	-	-	Dual Vth technique	Area overheads, delay may increase	Improved performance, reduced leakage power	Read SNM is improved by 2 times as compared to 6T SRAM, Leakage power is reduced by 57%
Birla Shilpi, Shukla Neeraj Kr., Pattanaik Manisha, Singh R.K., "Device and Circuit Design Challenges for Low Leakage SRAM for Ultra Low Power Applications,"[41]	90 CMOS	-	-	-	0.5	A data protection NMOS transistor is added.	1)write-write margin decreases with decreasing Vdd. 2)Read - storage data destruction	Vdd min-440mV, Access time-20ns, Better cell performance, Improved write margin	It may achieve high speeds,Leakage power is reduced by 21%
Yadav Monika, and Akashe Shyam, "New Technique For Reducing Sub-Threshold Leakage In SRAM,"[42]	180 CMOS	-	-	-	1.8	Sense Amplifiers	Layout optimization	Lower leakage current and power consumption	Area overhead increases by 16%, 47.5% better power saving
Takeda Koichi, Hagihara Yasuhiko, Aimoto Yoshiharu, Nomura Masahiro, Nakazawa Yoetsu, Ishii Toshio, and Kobatake Hiroyuki, "A Read-Static-Noise-Margin-Free SRAM Cell for Low-VDD and High-Speed Applications,"[43]	90 CMOS	-	-	-	0.5	Read-static-noise-margin-free SRAM cell	Leakage current increases with temperature	Low V_{dd} and high speed operation. Smaller area, SNM is improved	Area is 23% smaller Access time is 20ns
P Rajeev Anand., and P Chandra Sekhar., "Reduce Leakage Currents in Low Power	90 CMOS	9.738	0.000041600	-	1.0	Dual-VTH and transmission gate technique	Read Access time increases	Leakage current decreases, reduced static power dissi-	Leakage current=133nA, gate current leakage reduces by 58%,

SRAM cell Structures,"[44]								pation	static noise margin reduces by 10%

TABLE 8: THE 8T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Kim Tea-Hyoung, Liu J., and Kim C.H., "An 8T subthreshold SRAM Cell Utilizing Reverse Short Channel Effect for Write Margin and Read Performance Improvement,"[45]	130CMOS	-	0.0000063648	-	1.2	Reverse short channel effect	Leakage current increases, gate capacitance increases	Improved read and write margin, reduced threshold voltage	52% speedup , area overhead 20%, Ion/Ioff improved from 169 to 271, 3x longer channel length, no extra circuitary required
Verma N., and Chandrakasan A.P., "A 256 kb 65 nm 8T Subthreshold SRAM Employing Sense-Amplifier Redundancy,"[46]	65 CMOS	2.2	-	0.025	0.35	Sense amplifier redundancy	Increased device sizing and its statistical offset	High density, minimum operating voltage,more read write stability, low leakage power dissipation	Leakage power saving 10x, array size (256x128),30% area overhead
Wang Bo, Zhou Jun, and Kim Tony T., "Maximization of SRAM Energy Efficiency Utilizing MTCMOS Technology,"[47]	65 CMOS	-	-	-	0.4	Multi Threshold CMOS technology	Read,write delays may increase.	High energy efficiency, better performance	Array structure-256 rows x 128 columns, 33% incease in energy efficiency.
Kwong Joyce, Ramadass Yogesh K., Verma Naveen, and Chandrakasan Anantha P., "A 65 nm Sub-Vt Microcontroller With Integrated SRAM and Switched Capacitor DC-DC Converter,"[48]	65 CMOS	-	-	-	0.5	Timing process,subVt microcontroller with sub threshold memory	Area may increase	Leakage power and energy is reduced, improved stability	Array size-128kb, 1uW standby power at 300 mV, dc-dc converter achieves 75% efficiency Energy = 27.2 pJ

Liu Zhiyu and Kursun Volkan, "Characterization of a Novel Nine-Transistor SRAM Cell,"[40]	65 CMOS	-	-	-	-	Alternative communication channel (composed of a separate read bitline and the transistor stack) used for reading the data from the cell	Area over-head,delay may increase	Improved data stability	It may achieve high speeds. Leakage power is reduced by 23%.
Jain Sanjeev K., and Agarwal P., "A Low Leakage and SNM Free SRAM Cell Design in Deep Sub micron CMOS Technology[49]	90 CMOS	-	-	-	1.1	1 transistor reduces gate leakage and other makes cell SNM free.	Degradation in read access time when read = '0'	Reduction in gate leakage power. Cell area increases.	Total leakage reduced by 50.2%. SNM free when read = logic 0. SNM improved by 2.2 times. Increase in cell area is 30%.

TABLE 9: THE 9T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Ramani Ramnath Arun, and Choi Ken, "A Novel 9T SRAM Design in Sub-Threshold Region,"[50]	45 HSPICE	-	-	-	0.3	Sub threshold technique	Degradation in performance	Leakage power reduction, improved read ,write margin	Saving of PDP (write)- 2.80% <7T SRAM, 4.48 % < 8T SRAM , 5.64% <9T SRAM 8.5 % <11T SRAM. (read)- 44.8 % <7T SRAM 66.18 % <9T SRAM
Razavipour G., Kusha Afzali A., and Pedram M., "Design and Analysis of Two Low Power SRAM Cell Structures,"[51]	45 HSPICE	-	-	-	0.8	Dual Vth technique	Access time increases	Reduced static power dissipation and high performance	1st cell-Gate leakage current decreases by 66%, Ideal power decreases by 58%, 2nd cell--Gate leakage current decreases by 27%, Ideal power decreases by 37%, Channel length-pmos=0.4um,NMOS=0.2um

Mali Madan, Dr. Sutaone M.S., Bhalerao Mangesh, and Tak Shital, "Deep Submicron Implementation of Gating Transistor Power Saving Technique for Power Optimized Code Book SRAM,"[52]	250 SPICE	-	-	-	0.6	Attachement of extra row and column to SRAM	Area increases with decrease in power	Improved reliability, Access time, power dissipation is reduced ,	Access time reduces by 2ns, array size-256*8 , density -32kb, bit line length-1mm max, no metal layers-3, Power Dissipation reduced to 13%
Masuda Chotaro, Hirose Tetsuya, Matsumoto Kei, Osaki Yuji, Kuroki Nobutaka, and Numa Masahiro, "High Current Efficiency Sense Amplifier Using Body-Bias Control for Ultra-Low-Voltage SRAM,"[53]	350 SPICE	-	-	0.00333	0.5	current latch sense amplifier with a current-reuse technique	Power dissipation may increase	High speed pre charging, improved performance, small overhead	pre-charge time decreased by 86.9% , power dissipation increased by 8.6%,
Clark Lawrence T., Morrow Michael and Brown William, "Reverse-Body Bias and Supply Collapse for Low Effective Standby Power,"[54]	130 CMOS	165	1250000000000	0.032	1	Reverse body bias (RBB), voltage collapse technique	Area may increase	Low power dissipation, high efficiency, cost remains same	Easy to design RBB, density-34kb,83% stand by power reduction
Liu Zhiyu and Kursun Volkan, "Characterization of a Novel Nine-Transistor SRAM Cell,"[40]	65 CMOS	-	-	2000	1	Two separate data access mechanisms for the read and write operations.	Area may increase.	Improved data stability and leakage power reduction.	It may be used for high speed circuits. leakage power is reduced by 51%.

Singh R., Pattanaik M., and Shukla N., "Characterization of a Novel Low-Power SRAM Bit-Cell Structure at Deep Sub-Micron CMOS Technology for Multimedia Applications,"[55]	45 CMOS	-	-	-	0.8	IP3 SRAM bit-cell	Area and performance	Reduced power dissipation, Improved stability	tOX = 2.4 nm, Vthn = 0.224 V, Vthp = 0.24V at T = 27°C.during write-IP3 cell demands 17.65% and 41.53% less power as compared to 6T and PP cells.

TABLE 10: THE 10T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Saripalli Vinay, Datta Suman, Narayanan Vijaykrishnan, and Kulkarni Jaydeep P., "Variation-Tolerant Ultra Low-Power Heterojunction Tunnel FET SRAM Design,"[56]	45 TCAD	-	-	-	<300mV	TFET (tunnel FET) Schmitt-Trigger (ST)-SRAM with Feedback mechanism	Stability issues	Improved read/write noise margins, lowenergy, improved performance, can operate at low Vcc.	Improved variation tolerance, 1.2x reduction in dynamic energy, 13x reduction in leakage power
Calhounand Benton Highsmith and Chandrakasan Anantha P., "A 256-kb 65-nm Sub-threshold SRAM Design for Ultra-Low-Voltage Operation,"[57]	65 CMOS	3.28	-	0.475	0.3	Separate read and write word line	Speed may decrease	Improved cell stability, better noise margins, power and energy saving	It saves 2.5x and 3.8x in leakage power by scaling from 0.6v to 0.4v
Ebrahimi Amir, Kargaran Ehsan and Golmakani Abbas,"Design and Analysis of Three New SRAM Cells,"[58]	130 HSPICE	9.37	-	-	0.32	Separate read and write word line	Area overheads	Better SNM, reduced leakage current	512 cells per bit line and 128 column cell array is achieves better read and write

Lo Cheng-Hung and Huang Shi-Yu,"P-P-N Based 10T SRAM Cell for Low-Leakage and Resilient Subthreshold Operation,"[59]	90 CMOS	-	-	0.9	0.32	Cross coupled P-P-N inverter pair	Area overheads	Low cell leakage, high noise immunity, ability to operate at low voltage, high density	High immunity to data dependent bit line leakage
Moradi Farshad , Wisland Dag T., Mahmoodi Hamid, Berg Yngvar, and Cao. Tuan Vu, "New SRAM Design Using Body Bias Technique for Ultra Low Power Applications,"[60]	65	-	-	-	0.3	Body biasing technique	Area overheads may increase	Low power dissipation, ultra supply voltage scaling, SNM improvemnt	Static noise margin is improved by 15%, Improvement in SNM of READ cycle-22%

TABLE 11: THE 11T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Moradi Farshad, Wisland Dag.T., Aunet Snorre, Mahmoodi Hamid and Cao Tuan Vu, "65nm Sub-Threshold 11T-SRAM for Ultra Low Voltage Applications,"[61]	65 CMOS	-	-	-	0.2	Boost capacitor (CB) is used	Area may increase	Higher SNM and higher speed	Area overhead between 22 -28%, 4x improvement in read speed
Ebrahimi Amir, Kargaran Ehsan and Golmakani Abbas,"Design and Analysis of Three New SRAM Cells,"[58]	130 CMOS	6.29	-	-	0.27	Separate read and write word line	Area overheads	Better SNM, reduced leakage current	512 cells per bit line and 128 column cell array is achieves better read and write

Singh Ajay Kumar, Prabhu C.M.R., Pin Soo Wei and Hou Ting Chik, "A Proposed Symmetric and Balanced 11-T SRAM Cell for lower power consumption,"[62]	250 CMOS	-	-	-	2.5	Two tail transistors are used	Write access delay increased	Low circuit activity factor, Low active power density, reduced power consumption	Consumes 40% less average power, 7% slower during write operation
Lin Sheng, Kim Yong-Bin, and Lombardi Fabrizio, "A 11-Transistor Nanoscale CMOS Memory Cell for Hardening to Soft Errors,"[63]	32 CMOS	-	0.3764	-	0.9	Hardening approach	Speed and stability issues	Power delay product reduction. soft error tolerance improved	Superior resistance to soft errors, high performance
Chiu Yi-Wei, Hu Yu-Hao, Tu Ming-Hsien, Zhao Jun-Kai, Jou Shyh-Jye and Chuang Ching-Te, "A 40 nm 0.32 V 3.5 MHz 11T Single-Ended Bit-Interleaving Subthreshold SRAM with Data-Aware Write-Assist,"[64]	40 CMOS	-	-	3.5	0.32	Bit interleaving with data aware power cut off	Area overhead may increase	Improved write ability, can work at very low Vdd	Leakage power=13.5uW Switching energy=0.49pJ

TABLE 12: THE 12T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Mall Ambrish, Singh Suryabhan Pratap, Mishra Manish and Srivastava Geetika,"Analysis Of 12T SRAM CELL For Low Power Application,"[65]	45 CMOS	-	-	-	0.4	Data retention p gated, Series connected tail transistors	Area overheads may increase	Low power dissipation, reduced leakage current, low energy consumption	Transistor width=100nm, Power reduction by 45.94%

Chen Hu, Jun Yang, Meng Zhang and Xiulong Wu, "A 12T subthreshold SRAM Bit-cell for Medical Device Application," [66]	130 CMOS	-	-	-	0.4	Schmitt Trigger based SRAM	Robustness issues may arrive	High stability, more robustness	Power consumption reduces to 16%, 30.2% grater hold margin, 45% better SNM
Shayan Md, Singh Virendra, Singh Adit D and Fujita Masahiro, "SEU Tolerant Robust Memory Cell Design,"[67]	130 CMOS	-	-	-	1.2	SEU(single event upset) Tolerant SRAM	Reliability may reduce, area overheads may increase	High robustness, high performance, more economical	62x increase in Qcritical , It does not flip transient pulse ,α=0.2ns,β=0.05ns

TABLE 13: THE 13T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Sriram K V, Ranganna Ramappa Naik, Pavan Nandan S G and Kendaganna Swamy, "Design Of Low Power 64-Bit SRAM Using 13T Cell,"[68]	180 CMOS	283.33	-	-	1.1	Single read/write architecture, Stack technique	Area overheads may increase	High performance, improved noise margin, low power consumption	Power consumption-static=283.14uW dynamic=161.273uw Static noise margin-read SNM=0.70v write SNM=0.685v

TABLE 14: THE 14T SRAM BIT-CELL TOPOLOGY

Author & Title	Technology (nm)	Power (μW)	Area (mm^2)	Freq (MHz)	Vdd (V)	Methodology	Trade offs	Achievements	Comments
Fujiwara Hidehiro, Okumura Shunsuke, Iguchi Yusuke, Noguchi Hiroki, Kawaguchi Hiroshi and Yoshimoto Masahiko, "A 7T/14T Dependable SRAM and Its Array Structure to Avoid Half Selection,"[69]	65 CMOS	-	-	-	0.26	Quality of bit	Larger β ratio, SNM may increase	Improved reliability, speed. Read and write operations are improved	SRAM works in 3 modes-normal, high speed, dependable

Yoshimoto Shusuke, Amashita Takuro, Okumura Shunsuke, Yamaguchi Kosuke, Yoshimoto Masahiko, and Kawaguchi Hiroshi, "Bit Error and Soft Error Hardenable 7T/14T SRAM with 150-nm FD-SOI Process,"[70]	150 TCAD	-	-	-	0.1	FD-SOI	Between area (cost) and reliability	Improved BER (Bit Error Rate), SER (Soft Error Rate) and reliability. Improved minimum operating voltage	Alpha-induced SER suppressed by 80% Neutron-induced SER decreased by 34.4% Qcrit increased by 10-70% 14Tsuperior than 7T
Nakata Yohei, Ito Yasuhiro, Sugure Yasuo, Oho Shigeru, Takeuchi Yusuke, Okumura Shunsuke, Kawaguchi Hiroshi, and Yoshimoto Masahiko, "Model-Based Fault Injection for Failure Effect Analysis– Evaluation of Dependable SRAM for Vehicle Control Units,"[71]	65 CMOS	-	-	-	0.4-0.8	Fault Injection System	Dependability of SRAM affects dependability of processor system	System level dependability improves.	Area overhead is 11% greater. Has 2 modes – normal mode and dependable mode. *Vmin* improved by 0.05–0.15 V
Jinwook Jung, Yohei Nakata, Shunsuke Okumura, Hiroshi Kawaguchi, and Masahiko Yoshimoto, "256-KB Associativity-Reconfigurable Cache with 7T/14T SRAM for Aggressive DVS Down to 0.57 V,"[72]	65 CMOS	-	-	-	0.115	Associativity-reconfigurable cache. Consists of pair of cache ways. 2 pmos transistors are added	Performance decrease. area overhead is increased	Reliability enhance	Possesses scalable characteristic of reliability. Area overhead increased by 1.91% and 5.57% in 32-KB and 256-KB caches, It has 2 modes-normal mode and dependable mode

Jinwook Jung, Yohei Nakata, Shunsuke Okumura, Hiroshi Kawaguchi, and Masahiko Yoshimoto, "A Variation-Aware 0.57-V Set-Associative Cache with Mixed Associativity Using 7T/14T SRAM,"[73]	65 CMOS	-	2.04	-	0.57 in dependable mode	Induced defective SRAM cells, 2 pmos transistors are added andmixed associativity scheme is used	Area overhead, Don't have sufficient operating margins	Minimum operating voltage (*Vmin*) is reduced, reliability improves	Reduced *Vmin* by 80 mV within 7.81% capacity and 5.22% area overhead. It has 2 modes - normal mode and dependable mode
Yamaguchi Kosuke, Okumura Shunsuke, Yoshimoto Masahiko, and Kawaguchi Hiroshi, "0.42-V 576-kb 0.15-µm FD-SOI SRAM with 7T/14T Bit Cells and Substrate Bias Control Circuits for Intra-Die and Inter-Die Variability Compensation,"[74]	0.15 FD-SOI	-	-	-	0.42	FD-SOI substrate bias control mechanism.	Process variations may affect the system.	Maximizes the operating margin, retention voltage is reduced	Two operating modes - normal mode and dependable mode. Minimum retention is reduced to 0.28 V
Nakata Yohei , Okumura Shunsuke , Kawaguchi Hiroshi , and Yoshimoto Masahiko, "0.5-V Operation Variation-Aware Word-Enhancing Cache Architecture Using 7T/14T hybrid SRAM," [75]	65	-	-	-	0.5	Variation aware word enhancing scheme	Extra control lines are required	Improved reliability and control lines, Low power consumption	Suitable for dynamic voltage and frequency scaling(DVFS), Power reductions are 90% and 65%

Conclusion

In this paper a comparison on SRAM-Bit Cell based on different technology, cell type and analysis of various design techniques is done. In Dual V^{th} technique both leakage power and performance are improved with an area overhead and speed penalty. The MTCMOS offers low leakage power consumption with stronger stability at the cost of additional transistors. In Body biasing threshold voltage is modified which reduces leakage power but at the cost of stability. Sense amplifier offers low leakage power dissipation with increased device sizing and layout optimization. In Sub threshold both leakage power, read and write margins are improved at the cost of performance degradation. If speed is increased, area also increases. If high robustness is obtained, then noise margins increases.

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